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CBCS SCHEME

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BEC302

Third Semester B.E./B.Tech. Degree Examination, June / July 2026
Digital System Design Using Verilog

Time: 3 hrs. Max. Marks: 100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. M : Marks , L: Bloom's level , C: Course outcomes.

		Module – 1	M	L	C
Q.1	a.	What are Combinational Circuits? Explain combinational circuits with block diagram.	04	L2	CO1
	b.	Develop minimal expression using K – map for the following incompletely specified function. f (a, b, c, d) = Σm (0, 1, 4, 6, 7, 9, 15) + Σd (3, 5, 11, 13) and draw the circuit diagram using basic gates.	06	L3	CO1
	c.	Define canonical form representation and solve the following equation using canonical form. i) D = f (a, b, c) = $ab^1 + ac^1 + bc$ ii) K = f (w, x, y, z) = $w^1x + yz^1$.	10	L3	CO1
		OR			
Q.2	a.	Define K – map, solve the following using K – map i) K = f (w, x, y, z) = Σm (0, 1, 4, 5, 9, 11, 13, 15) ii) D = f (a, b, c, d) = Σm (0, 1, 2, 4, 5, 6, 8, 9, 12, 13, 14)	10	L3	CO1
	b.	Develop all the prime implicants of the following Boolean function using Quine – Mccluskey method. f (a, b, c, d) = Σ (0, 2, 3, 5, 8, 10,11). Verify the result using K –map technique.	10	L3	CO1
		Module – 2			
Q.3	a.	Explain binary Adder's with K – map and logical representation of equations for SUM and CARRY.	06	L2	CO2
	b.	Explain Look – Ahead carry adder with neat diagram and relevant expression.	06	L2	CO2
	c.	A combinational circuit is defined by the functions f_1 = Σm (3, 5, 7), f_2 = Σ m (4, 5, 7). Implement the circuit with a programmable logic array having 3 inputs, 3 product terms and 2 outputs.	08	L3	CO2
		OR			
Q.4	a.	Draw the circuit for 3 to 8 decoder and explain.	06	L2	CO2
	b.	Design 2 – bit comparator using gates.	06	L2	CO2
	c.	Implement D = (w, x, y, z) = Σm (0, 1, 2, 4, 5, 7, 8, 9, 12, 13) using 8:1 MUX.	08	L3	CO2

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		Module – 3			
Q.5	**a.**	Draw and explain the logic diagram, functional table and timing diagram of master – slave JK flip flop.	**10**	**L2**	**CO3**
	b.	Explain 4 – bit binary ripple counter with logic diagram and timing diagram.	**10**	**L2**	**CO3**
		OR			
Q.6	**a.**	Develop characteristic equation for S – R and T flip flops with the help of function table and explain.	**06**	**L3**	**CO3**
	b.	What are Registers? Explain any two classification of Data Movement registers with neat block diagram.	**06**	**L2**	**CO3**
	c.	Design Synchronous MOD – 6 counter using clocked JK flip flops for sequences: 0 – 2 – 3 – 6 – 5 – 1	**08**	**L3**	**CO3**
		Module – 4			
Q.7	**a.**	Describe different styles of HDL descriptions with an example for each.	**08**	**L2**	**CO4**
	b.	Write Verilog code for full Adder using dataflow description.	**06**	**L2**	**CO4**
	c.	Write a note on Arithmetic and shift, operators with example.	**06**	**L2**	**CO4**
		OR			
Q.8	**a.**	Define HDL and types of HDL. Give structure of verilog module with example.	**06**	**L2**	**CO4**
	b.	Explain Verilog logical operators with example.	**06**	**L2**	**CO4**
	c.	i) Write a note an Verilog Data type ii) Write a Verilog code for 8 × 1 MUX	**08**	**L2**	**CO4**
		Module – 5			
Q.9	**a.**	Write a Verilog code for 2 × 1 MUX using ELSE STATEMENT.	**06**	**L2**	**CO5**
	b.	Explain structural description with an example.	**08**	**L2**	**CO5**
	c.	Write a structural description of 3 – bit ripple carry adder.	**06**	**L2**	**CO5**
		OR			
Q.10	**a.**	Write a note on Structure of Behavioural Description with an example.	**08**	**L2**	**CO5**
	b.	Write a note on Signal Assignment and Variable Assignment with an example.	**06**	**L2**	**CO5**
	c.	Write a note on sequential statement with an example.	**06**	**L2**	**CO5**

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